



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,026	08/14/2000	Paul A. Farrar	M4065.0082/P082-A	8833

24998 7590 04/17/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP  
2101 L STREET NW  
WASHINGTON, DC 20037-1526

EXAMINER

PAREKH, NITIN

ART UNIT PAPER NUMBER

2811

DATE MAILED: 04/17/2003

//

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/638,026

Applicant(s)

FARRAR, PAUL A.

Examiner

Nitin Parekh

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 February 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 40,43-51,68-70,72,74 and 75 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 40,43-51,68-70,72,74 and 75 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other.

Art Unit: 2811

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 40, 43-49, 68, 69, 71, 72, 74 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) in view of Svetkoff et al. (US Pat. 6249347).

Regarding claim 40, Yamamoto discloses a semiconductor device/an integrated circuit (IC) chip on a semiconductor substrate/silicon wafer (21/22 in Fig. 7) comprising:

- a semiconductor structure having a metal contact (23 in Fig. 7) formed on the surface thereof
- a first insulator layer (24/41 in Fig. 7) overlying the metal contact
- a metal pad/interconnection (50 in Fig. 7) overlying the first insulator layer and in contact with the metal contact, the metal pad being partially overtop of the metal contact and comprising a stack of four different metals/levels including zinc, nickel, copper and gold (43, 44, 45, 46A, 46B, 50, etc. in Fig. 7; Col. 5, line 9-35)

Art Unit: 2811

- a second insulator layer (47 in Fig. 7) overlying the metal pad
- the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) in the first insulator, and
- solder contact/ball (48 in Fig. 7) formed in the second insulator layer and in contact with the metal pad, the solder contact/ball extending from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (Fig. 7)

(Fig. 7; Col. 6, line 40- Col. 7, line 5; Col. 4-8).

Yamamoto fails to specify the diameter of the solder contact being less than 100 microns.

Svetkoff et al. teach a miniature/micro ball grid array (BGA) device using solder balls (200 in Fig. 11) having a typical range of 10-300 microns to achieve the increased interconnect density and very fine geometries/ground rules (Col. 11, lines 27-37; Col. 1 and 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device.

Art Unit: 2811

Regarding claims 43 and 44, Yamamoto teaches substantially the entire claimed structure as applied to claim 40, except the solder contacts having the diameter of less than 10 microns or that being approximately 2 microns respectively.

The determination of parameters such as size/dimension, range and shape of the metal/solder contacts and metallization structure including diameter, pitch/spacing, pad dimension, number/thickness of an insulating layer, number/diameter of vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired I/O density, line width/ground rules, performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 10 microns, approximately 2 microns or having a range of 2-100 microns as taught by Svetkoff et al. so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device.

Regarding claim 45, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, including the metal contact being connected to the metal pad by a via hole formed in the first insulator.

Art Unit: 2811

Regarding claim 46, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, including the solder contacts extending from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator.

Regarding claim 47, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, including the metal pad being partially overtop of the metal contact.

Regarding claim 48, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, including the semiconductor device being the IC chip.

Regarding claim 49, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, including the semiconductor device being an IC wafer.

Regarding claim 68, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, except the first insulating layer being 2 microns thicker than the metal contact.

Yamamoto further teaches the first insulating layer being 10-50 microns thick (41 in Fig. 7; Col. 4, line 39) and as shown in Fig. 7, the insulating layer being approximately

Art Unit: 2811

2-3 times thicker than the metal pad/contact (23 in Fig. 7) or more than 2 microns thicker than the metal pad/contact.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. and the first insulating layer being 2 microns thicker than the metal contact so that the interconnect density and passivation/insulation integrity can be improved in Yamamoto's device.

Regarding claim 69, Yamamoto teaches substantially the entire claimed structure as applied to claim 40 above, including the metal pad comprising a stack of four different metals.

Regarding claim 71, Yamamoto teaches substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter between 2-100 microns.

Regarding claim 72, Yamamoto teaches substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of approximately 2 microns.

Art Unit: 2811

Regarding claim 74, Yamamoto teaches substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of less than 50 microns.

Regarding claim 75, Yamamoto teaches substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of less than 25 microns.

3. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) and Svetkoff et al. (US Pat. 6249347) as applied to claim 40 above, and further in view of the admitted prior art (APA).

Regarding claim 50, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, except the device being bonded to a module substrate.

The APA teaches a semiconductor device being bonded to a module substrate or a circuit board (specification page 2; Fig. 1-3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. and the device being bonded to the module



Art Unit: 2811

substrate as taught by the APA so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto and Svetkoff et al's device.

Regarding claim 51, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 50 above, including the device being bonded to a circuit board.

4. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) and Svetkoff et al. (US Pat. 6249347) as applied to claims 40 and 69 above, and further in view of Takashi et al. (Japanese Pat. 408236938).

Regarding claim 70, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 69 above, except using Zirconium as one of the four metals in the stack.

Takashi et al. teach using metal pad/conductor (114 in Fig. 1-4) comprising metals such as copper and zirconium (see abstract in English Translation).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. the metal pad comprising a stack of four different metal levels comprising zirconium, nickel, copper and gold as taught by Takashi et al.

Art Unit: 2811

so that the electrical parameters/properties of the interconnect can be improved and the device size/ground rules can be reduced in Yamamoto and Svetkoff et al's device.

***Response to Arguments***

5. Applicant's arguments with respect to claims 40, 43-51, 68-72, 74 and 75 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2811

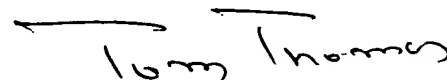
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP  
April 11, 2003



TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800